In the claims:

Please amend the claims as follows:

1. (Cancelled)

2. (Currently Amended) The method of claim ~~1~~ 5 wherein configuring the buffer responsive to the applied configuration signal comprises detecting an edge of the applied configuration signal.

3. (Currently Amended) The method of claim ~~1~~ 5 wherein configuring the buffer responsive to the applied configuration signal comprises detecting a level of the applied configuration signal.

4. (Currently Amended) The method of claim ~~1~~ 5 wherein applying the configuration signal on one of the first and second data signal nodes comprises:

selecting one of the data signal nodes to which the configuration signal is to be applied, wherein the selected data signal node determines a direction of operation of the buffer; and

applying the configuration signal to the selected data signal node.

5. (Currently Amended) A method of configuring a bidirectional buffer, the buffer including first and second data signal nodes and the method comprising:

applying a configuration signal on one of the first and second data signal nodes;

configuring the buffer responsive to the applied configuration signal; and

~~The method of claim 1 further comprises~~ applying a reset signal to disable the buffer prior to applying the configuration signal on one of the first and second data signal nodes.

6. (Currently Amended) The method of claim ~~1~~ 5 wherein the configuration signal comprises a series of pulses.

7. (Currently Amended) The method of claim ~~1~~ 5 wherein configuring the buffer responsive to the applied configuration signal comprises enabling the buffer to operate in a first direction with the first data signal node corresponding to an input node and the second data signal node corresponding to an output node.

8. (Cancelled)

9. (Currently Amended) A method of configuring a bidirectional buffer, the buffer including first and second data signal nodes and the method comprising:

applying a configuration signal on one of the first and second data signal nodes;

storing a first memory bit responsive to the applied configuration signal, the first memory bit having a first logic state;

enabling the buffer to operate in a first direction responsive to the stored memory bit;~~The method of claim 8 wherein storing a first memory bit responsive to the applied configuration signal comprises:~~

~~storing the first memory bit having a first logic state responsive to the applied configuration signal;~~ and

storing a second memory bit having a second logic state responsive to storing the first memory bit.

10. (Original) The method of claim 9 wherein the second memory bit has logic state that is the complement of the first logic state.

11. (Original) The method of claim 10 wherein storing a second memory bit having a second logic state responsive to storing the first memory bit

comprises maintaining the second memory bit at the complement of the first logic state responsive to storing the first memory bit.

12. (Original) A bidirectional programmable buffer, comprising:

a pair of cross-coupled buffer circuits, each buffer circuit including an enable input and the cross-coupled pair of buffer circuits having two data nodes; and

a detection and configuration circuit coupled to the enable inputs of the buffer circuits and coupled to the two data nodes, the detection and configuration circuit operable in a configuration mode to detect a configuration signal applied on one of the data nodes and to enable a corresponding one of the buffer circuits responsive to the detected configuration signal, and operable in a data mode to provide through the enabled buffer circuit a data signal applied on one of the data nodes responsive to the data signal being applied on the other of the data nodes.

13. (Original) The bidirectional programmable buffer of claim 12 wherein the detection and configuration circuit comprises:

a first edge-triggered storage circuit having a clock input coupled to one of the data nodes, an output coupled to the enable input of one of the buffer circuits, and an input, the first edge-triggered storage circuit operable responsive to an edge of a configuration signal applied on the clock input to provide on the output a signal having a complementary logic state of a signal on the input; and

a second edge-triggered storage circuit having a clock input coupled to the other one of the data nodes, an output coupled to the enable input of the other one of the buffer circuits and coupled to the input of the first edge-triggered storage circuit, and having an input coupled to the output of the first edge-triggered storage circuit, second edge-triggered storage circuit operable responsive to an edge of a configuration signal applied on the clock input to provide on the output a signal having a complementary logic state of a signal on the input.

14. (Original) The bidirectional programmable buffer of claim 13 wherein the first and second edge-triggered storage circuits each comprise:

a flip-flop; and

an inverter coupled between the output of each flip-flop and the input of the other flip-flop.

15. (Original) The bidirectional programmable buffer of claim 14 wherein each of the flip-flops further includes a reset input adapted to receive a reset signal.

16. (Original) The bidirectional programmable buffer of claim 12 wherein the detection and configuration circuit comprises:

a first level-triggered storage circuit having an output coupled to the enable input of one of the buffer circuits and having an input coupled to one of the two data nodes, the first level-triggered storage circuit operable responsive to a level of a configuration signal applied on the data node to provide an enable signal to the corresponding buffer circuit; and

a second level-triggered storage circuit having an output coupled to the enable input of the other one of the buffer circuits and having an input coupled to the other one of the two data nodes, the second level-triggered storage circuit operable responsive to a level of a configuration signal applied on the data node to provide an enable signal to the corresponding buffer circuit.

17. (Original) The bidirectional programmable buffer of claim 16 wherein each of the level-triggered storage circuits comprises:

a latch circuit having an input and having an output coupled to the enable input of the corresponding buffer circuit, the latch circuit operable to latch a signal on the output to a first logic state that is the complement of the logic state of a signal applied on the input; and

first, second, and third controllable switches having signal terminals coupled respectively between a supply voltage source and a reference voltage source, each of the switches having a control terminal and wherein the control terminal of the first switch is adapted to receive a reset signal and the control terminal of the second switch is coupled to the corresponding data node, and the input of the latch circuit being coupled to a node defined by the interconnection of the

signal terminals of the first and second switches, and wherein the control terminal of the third switch is adapted to receive the signal on the input of the latch circuit contained in the other level-triggered storage circuit.

18. (Original) The bidirectional programmable buffer of claim 17 wherein the latch circuit comprises a pair of cross-coupled inverters.

19. (Original) The bidirectional programmable buffer of claim 17 wherein the first controllable switch comprises a PMOS transistor and wherein the second and third controllable switches each comprise an NMOS transistor.

20. (Original) The bidirectional programmable buffer of claim 17 further comprising:

first and second series-connected controllable reset switches coupled between one of the data nodes and a reference voltage source, each of the switches having a respective control terminal adapted to receive the signal on the input of the latch circuit in one of the level-triggered storage circuits; and

third and fourth series-connected controllable reset switches coupled between the other one of the data nodes and the reference voltage source, each of these switches having a respective control terminal adapted to receive the signal on the input of the latch circuit in one of the level-triggered storage circuits.

21. (Original) A semiconductor circuit, comprising:

a plurality of bidirectional programmable buffers, each buffer including,

a pair of cross-coupled buffer circuits, each buffer circuit including an enable input and the cross-coupled pair of buffer circuits having two data nodes; and

a detection and configuration circuit coupled to the enable inputs of the buffer circuits and coupled to the two data nodes, the detection and configuration circuit operable in a configuration mode to detect a configuration signal applied on one of the data nodes and to enable a corresponding one of the buffer circuits responsive to the detected configuration signal, and operable in a data mode

to provide through the enabled buffer circuit a data signal applied on one of the data nodes responsive to the data signal being applied on the other of the data nodes; and

logic circuitry coupled to at least some of the buffers and operable to execute a desired function.

22. (Original) The integrated circuit of claim 21 wherein the semiconductor comprises a memory device.

23. (Original) An electronic system, comprising:

processing circuitry coupled to an integrated circuit, the integrated circuit including a plurality of bidirectional bidirectional programmable buffers and each buffer including,

a pair of cross-coupled buffer circuits, each buffer circuit including an enable input and the cross-coupled pair of buffer circuits having two data nodes; and

a detection and configuration circuit coupled to the enable inputs of the buffer circuits and coupled to the two data nodes, the detection and configuration circuit operable in a configuration mode to detect a configuration signal applied on one of the data nodes and to enable a corresponding one of the buffer circuits responsive to the detected configuration signal, and operable in a data mode to provide through the enabled buffer circuit a data signal applied on one of the data nodes responsive to the data signal being applied on the other of the data nodes.

24. (Original) The electronic system of claim 23 further comprising:

an input device coupled to the processing circuitry;
an output device coupled to the processing circuitry; and
a data storage device coupled to the processing circuitry.

25. (Original) The electronic system of claim 23 wherein the system comprises a computer system.